IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 4 with the following:

This application is a Divisional of U.S. Application Serial No. 10/607,301 filed June 27, 2003; which is a Divisional of U.S. Application Serial No. 10/279,910 filed on October 25, 2002; which is a Divisional of U.S. Application Serial No. 09/902,168 filed on July 11, 2001, hereby incorporated by reference as to its entirety. This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2000-210474, filed July 11, 2000, the entire contents of which are incorporated herein by reference.

Please delete the paragraphs beginning on page 9, line 24 to page 12, line 16 as follows:

~~Accordingly, an object of this invention is to provide a semiconductor memory device in which the hierarchical word line system or hierarchical block selecting line system can be applied to reduce the chip area and lower the process cost without increasing the number of interconnection layers.~~

~~Further, another object of this invention is to provide a semiconductor memory device capable of attaining high integration, further reducing the chip area and lowering the process cost while maintaining simplification of the manufacturing method and the random access function.~~

~~The above object can be attained by a semiconductor memory device comprising a memory cell array which includes a plurality of sub-arrays, a plurality of sub-rows decoders provided between the plurality of sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one end side of the plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of the main row decoder to the sub-row decoders; wherein the plurality of sub-arrays each include the plurality of sub-word lines, a plurality of bit~~

~~lines, a plurality of plate lines and a plurality of memory cell blocks, the plurality of the sub-arrays are arranged in the sub-word line direction, the memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of the series-connected portion, one end of each of the memory cell blocks is coupled to a corresponding one of the bit lines, the other end thereof is connected to a corresponding one of the plate lines, the gate terminal of a cell transistor is connected to a corresponding one of the sub-word lines, the memory cell includes the cell transistor and a ferroelectric capacitor connected between the source and drain terminals of the cell transistor, and a metal interconnection used for parallel connection of the cell transistor and the ferroelectric capacitor is formed of a metal interconnection layer formed at the same level as the main-block selecting lines.~~

~~Further, the above object can be attained by a semiconductor memory device comprising a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between the plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one end side of the plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of the main row decoder to the sub-row decoders; wherein the plurality of sub-arrays each include the plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, the plurality of the sub-arrays are arranged in the sub-word line direction, a metal interconnection used for forming the plate lines and a metal interconnection used for forming the main-block selecting lines are formed of metal interconnection layers at the same level, the memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of the series-connected portion, one end of each of the memory cell~~

~~blocks is coupled to a corresponding one of the bit lines, the other end thereof is connected to a corresponding one of the plate lines, the gate terminal of each cell transistor is connected to a corresponding one of the sub-word lines, and the memory cell includes the cell transistor and a ferroelectric capacitor connected between the source and drain terminals of the cell transistor.~~

Please replace the paragraph from page 12, line 17, through page 13, line 24, with the following:

~~Further, the above object can be attained by~~ According to an aspect of the present invention, there is provided a semiconductor memory device comprising a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between the plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed of one-end side of the plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of the main row decoder to the sub-row decoders; wherein the plurality of sub-arrays each include the plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, the plurality of the sub-arrays are arranged in the sub-word line direction, a metal interconnection used for forming the plate lines and a metal interconnection used for forming the main-block selecting lines are formed of metal interconnection layers at the same level, the memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of the series-connected portion, one end of each of the memory cell blocks is coupled to a corresponding one of the bit lines, the other end thereof is connected to a corresponding one of the plate lines, the gate terminal of each cell transistor is connected to a corresponding one of the sub-word lines, the memory cell includes

the cell transistor and a ferroelectric capacitor connected between the source and drain terminals of the cell transistor, and a metal interconnection used for parallel connection of the cell transistor and the ferroelectric capacitor is formed of a metal interconnection layer formed at the same level as the plate lines and the main-block selecting lines.

Please delete the paragraphs from page 13, line 25, through page 15, line 24, as follows:

~~Further, the above object can be attained by a semiconductor memory device comprising a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between the plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one end side of the plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of the main row decoder to the sub-row decoders; wherein the plurality of sub-arrays each include the plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, the plurality of the sub-arrays are arranged in the sub-word line direction, the memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of the series-connected portion, one end of each of the memory cell blocks is coupled to a corresponding one of the bit lines, the other end thereof is connected to a corresponding one of the plate lines, the gate terminal of each cell transistor is connected to a corresponding one of the sub-word lines, at least part of the main-block selecting lines is formed over the source, drain and gate electrode of the selection transistor, and the memory cell includes the cell transistor and a ferroelectric capacitor connected between the source and drain terminals of the cell transistor.~~

~~Further, the above object can be attained by a semiconductor memory device comprising a memory cell block having a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of the series-connected portion, wherein one end of the memory cell block on the selection transistor side is connected to a bit line and the other end thereof is connected to a plate line, the memory cell includes a cell transistor and a ferroelectric capacitor connected between the source and drain terminals of the cell transistor, a bottom electrode of the ferroelectric capacitor of the memory cell connected to the plate line is connected to a diffusion layer via a contact between the bottom electrode and the diffusion layer, and the diffusion layer is connected to the plate line formed of a metal interconnection layer via a contact between the diffusion layer and the metal interconnection.~~

~~Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.~~

Please delete the paragraph on page 15, beginning on line 26 to page 16, line 4 as follows:

~~The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently embodiments of the invention, and together with the general description given above and the detailed description of the embodiments given below, serve to explain the principles of the invention.~~

Please amend the paragraph on page 40, beginning on line 2, as follows:

As described above, ~~according to this invention~~ according to one aspect of this invention, the hierarchical word line system and hierarchical block selecting line system which can be easily

formed by use of nonvolatile plane transistors and realize high integration while the random access function can be maintained can be attained without increasing the number of interconnection layers, that is, raising the process cost, since the main-block selecting line for connecting the main row decoder to the sub-row decoder can be formed by use of the same interconnection layer as the plate interconnection and metal interconnection used between the memory cells in the cell block. Thus, the area of the decoder can be significantly reduced and the chip size can be reduced.